CLAIMS

1. A transistor, comprising,

a first conducting structure upon a substrate;

a second conducting structure upon said substrate, with the projection of said second conducting structure onto said substrate intersecting the projection of said first conducting structure onto said substrate;

a third conducting structure upon said substrate contacting with said first conducting structure, with the projection of said third conducting structure onto said substrate separated from said projection of said second conducting structure onto said substrate;

a fourth conducting structure upon said substrate contacting with said second conducting structure, with the projection of said fourth conducting structure onto said substrate separated from said projection of said first conducting structure onto said substrate, and said fourth conducting structure onto said substrate intersecting the projection of said third conducting structure onto said substrate; and

a fifth conducting structure upon said substrate, with the projection of said fifth conducting structure onto said substrate at least partly overlapping said projection of said fourth conducting structure onto said substrate and separated from said projection of said third, said first, and said second conducting structure onto said substrate.

2. The transistor as set forth in Claim 1, wherein said projection of said fifth and said second conducting structure onto said substrate being on the opposite sides of said projection of said third conducting structure onto said substrate.

3. The transistor as set forth in Claim 1, wherein said projection of said fifth conducting structure onto said substrate not contacting with the end of said projection of said fourth conducting structure onto said substrate not contacting with said second conducting structure.

4. The transistor as set forth in Claim 1, wherein said projection of said fifth conducting structure onto said substrate completely inside said projection of said fourth conducting structure onto said substrate.

5. The transistor as set forth in Claim 1, while said projection of said fifth conducting structure onto said substrate not completely inside said projection of said fourth conducting structure onto said substrate, said projection of said fifth conducting structure onto said substrate not contacting with the end of said projection of said fourth conducting structure onto said substrate not contacting with said second conducting structure.

6. The transistor as set forth in Claim 5, wherein the opposite two sides of said projection of said fourth conducting structure onto said substrate passed by said projection of said fifth conducting structure onto said substrate approximately parallel to one another at and near the intersecting area of said projection of said fourth and said fifth conducting structure.

7. The transistor as set forth in Claim 1, wherein the opposite two sides of said projection of said fifth conducting structure onto said substrate passed by said projection of said fourth conducting structure onto said substrate approximately parallel to one another at and near the intersecting area of said

projection of said fourth and said fifth conducting structure.

8. The transistor as set forth in Claim 1, wherein said projection of said fifth and said fourth conducting structure onto said substrate being approximately parallelograms.

9. The transistor as set forth in Claim 1, further comprising a semiconductor layer upon said substrate and electrically coupling with said third and said fifth conducting structure with the projection of said semiconductor layer onto said substrate completely inside said projection of said fourth conducting structure onto said substrate.

10. A transistor, comprising,

a first conducting structure upon a substrate;

a second conducting structure upon said substrate, with the projection of said second conducting structure onto said substrate intersecting the projection of said first conducting structure onto said substrate;

a third conducting structure upon said substrate contacting with said first conducting structure, with the projection of said third conducting structure onto said substrate completely inside said projection of said second conducting structure onto said substrate; and

a fourth conducting structure upon said substrate, with the projection of said fourth conducting structure onto said substrate separated from said projection of said first and said third conducting structure onto said substrate, said projection of said fourth conducting structure onto said substrate completely inside said projection of said second conducting structure onto said substrate; and said projection of said fourth conducting structure onto said

substrate approximately parallel to said projection of said third conducting structure onto said substrate.

11. The transistor as set forth in Claim 10, wherein the side of said projection of said fourth conducting structure onto said substrate approximately parallel to said projection of said third conducting structure onto said substrate far longer than the side of said projection of said fourth conducting structure onto said substrate approximately parallel to said projection of said first conducting structure onto said substrate.

12. The transistor as set forth in Claim 10, wherein said side of said projection of said fourth conducting structure onto said substrate approximately parallel to said projection of said third conducting structure onto said substrate at least seven times longer than said side of said projection of said fourth conducting structure onto said substrate approximately parallel to said projection of said first conducting structure onto said substrate.

13. The transistor as set forth in Claim 10, further comprising a fifth conducting structure upon said substrate contacting with said fourth conducting structure, with the projection of said fifth conducting structure onto said substrate separated from said projection of said first and said third conducting structure onto said substrate, said projection of said fifth conducting structure onto said substrate at least partly inside said projection of said second conducting structure onto said substrate, said projection of said fifth and said third conducting structure onto said substrate on the opposite sides of said projection of said fourth conducting structure onto said substrate, and the side of said projection of said fourth conducting structure onto said substrate facing

said projection of said fifth conducting structure onto said substrate only partly contacting with said projection of said fifth conducting structure onto said substrate.

14. The transistor as set forth in Claim 13, wherein the area of said projection of said fourth conducting structure onto said substrate far larger than that of the overlap between said projection of said fifth and said second conducting structure.

15. The transistor as set forth in Claim 10, further comprising a semiconductor layer upon said substrate electrically coupling with said third and said fourth conducting structure, with the projection of said semiconductor layer onto said substrate completely inside said projection of said second conducting structure onto said substrate.

16. A method forming transistors, comprising,

providing a wafer, with its surface separated into an array of a plurality of cell areas;

providing a first, a second, and a third mask, wherein the pattern of the first mask comprising a first line-shaped pattern and a first block-shaped pattern aside and contacting with said first line-shaped pattern, the pattern of the second mask comprising a second line-shaped pattern and a second block-shaped pattern aside and contacting with said first line-shaped pattern, and the pattern of the third mask a ring-shaped pattern;

forming a transistor pattern on a cell area using said first, said second, and said third mask, wherein the alignment error of any mask along the direction of the first line-shaped pattern being a first displaced position, the

alignment error of any mask along the direction of the second line-shaped pattern being a second displaced position, and said transistor pattern satisfying:

said pattern of said first mask partly overlapping said pattern of said second mask, resulting in that said first line-shaped pattern partly overlapping said second line-shaped pattern, said first block-shaped pattern partly overlapping said second block-shaped pattern, said first line-shaped pattern completely separated from said second block-shaped pattern, and said second line-shaped pattern completely separated from said first block-shaped pattern;

said pattern of said first mask completely separated from said pattern of said third mask; and

said pattern of said second mask partly overlapping said pattern of said third mask, resulting in that said ring-shaped pattern partly overlapping said second block-shaped pattern, said ring-shaped pattern completely separated from said second line-shaped pattern, and said overlap between said ring-shaped pattern and said second block-shaped pattern and said contacting part of said second line-shaped pattern and said second block-shaped pattern on the opposite sides of said overlap between said first block-shaped pattern and said second block-shaped pattern; and

repeating using said masks to form said transistor pattern on each cell area.

17. The method forming transistors as set forth in Claim 16, further comprising forming the pattern of a semiconductor layer as part of said transistor pattern, wherein said pattern of said semiconductor layer electrically coupling with said first block-shaped and said second block-shaped pattern, and said pattern of said semiconductor layer completely inside said second line-shaped pattern.

18. The method forming transistors as set forth in Claim 16, if said overlap between said ring-shaped and said second block-shaped being a first part pattern, then the distance between the side of said first part pattern facing said second block-shaped pattern and said second block-shaped pattern being larger than said first v, the distance between said side of said first part pattern facing said second block-shaped pattern and said second line-shaped pattern being larger than said first displaced position, and the distance between the side of said first block-shaped pattern facing said second line-shaped pattern and said second line-shaped pattern being larger than said first displaced position.

19. The method forming transistors as set forth in Claim 16, the distance between the side of said second block-shaped pattern facing said first line-shaped pattern and said first line-shaped pattern being larger than said second displaced position, the distance between the side of said ring-shaped pattern facing said first line-shaped pattern and said first line-shaped pattern being larger than said second displaced position

20. The method forming transistors as set forth in Claim 16, if said ring-shaped pattern having a second part pattern and a third part pattern both approximately parallel to said first line-shaped pattern, then the distance between said second part pattern and said second block-shaped pattern being larger than said second displaced position, and the distance between said third part pattern and said second block-shaped pattern being larger than said second displaced position.